TEMIC

TELEFUNKEN Semiconductors

TDA 4462

IF 1-Chip Processor (Video IF and Mono FM Sound IF)

Description

The TDA 4462 is a near alignment–free 1–chip video/ sound IF concept for TV–IF signal processing. The circuit processes all video IF signals with negative modulation and FM sound IF signals (mono FM intercarrier sound). With 5 V supply voltage the TDA 4462 is suitable for TV, VCR and Multimedia applications.

Features

- 5V supply voltage; low power consumption

- Minimum number of external components

- Active carrier generation by FPLL principle (frequency–phase–locked–loop) for true synchronous demodulation

- Very linear video demodulation, excellent pulse response and good intermodulation figures

- VCO circuit is operating on picture carrier frequency

- Alignment–free AFC without external reference circuit

- VIF–AGC with peak sync detection

- Tuner AGC with adjustable take over point

- Complete alignment–free PLL demodulator for FM-intercarrier sound IF signals (mono)

- Full SCART interface for video and audio signals

- Volume control by DC voltage

Package

28 pin shrink–dual–inline–plastic (SDIP 28) or
28 pin small outline plastic (SO 28)

Figure 1. Block diagram

94 8025

Preliminary Information
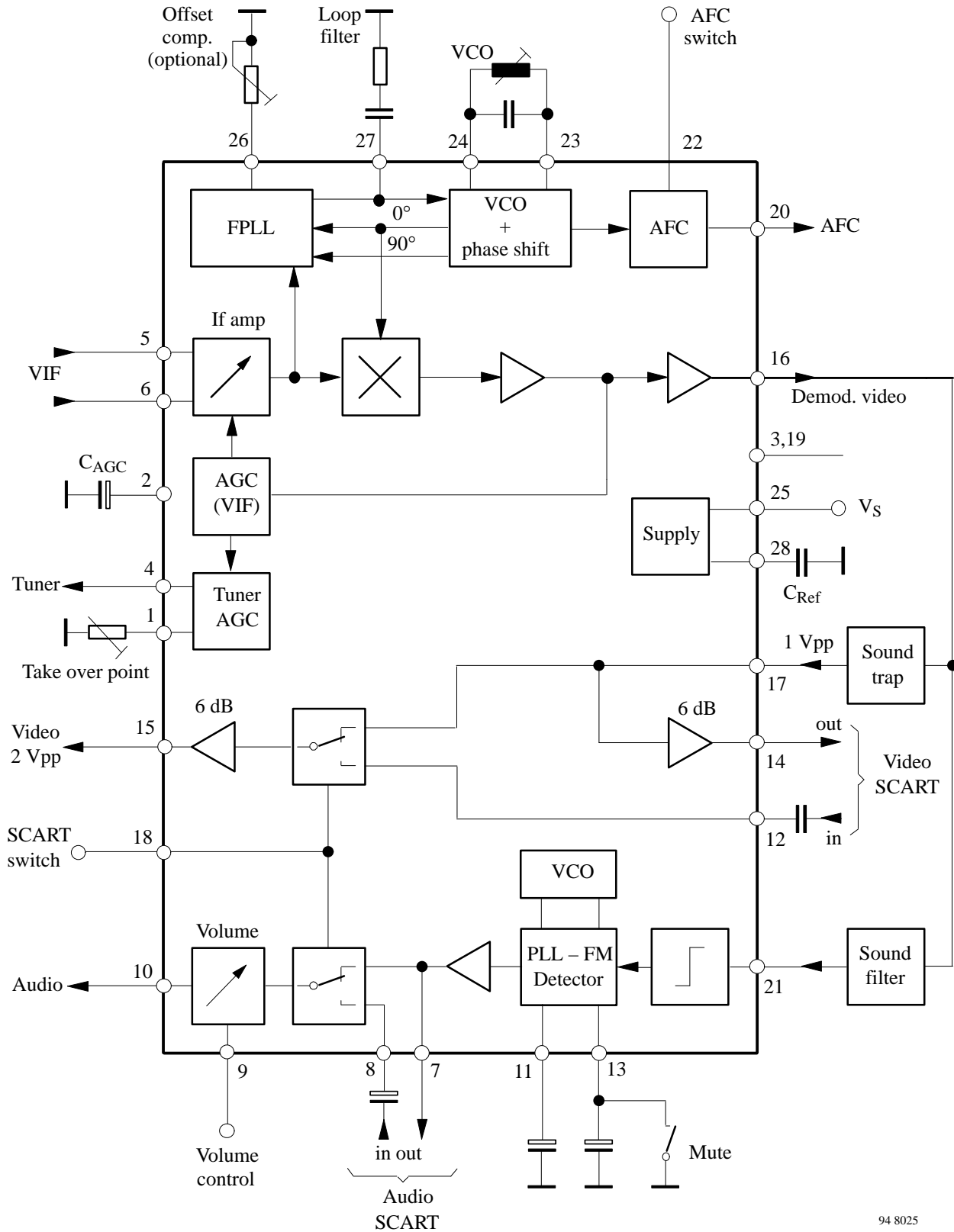
Circuit Description

Vision IF amplifier

The video IF signal (VIF) is fed through a SAW filter to the differential input (Pin 5–6) of the VIF amplifier. This amplifier consists of three AC–coupled amplifier stages. Each differential amplifier is gain controlled by the automatic gain control (VIF–AGC). Output signal of the VIF amplifier is applied to the FPLL carrier generation and the video demodulator.

Tuner– and VIF–AGC

At Pin 2 the VIF–AGC charges/discharges the AGC capacitor to generate a control voltage for setting gain of VIF amplifier and tuner in order to keep the demodulated video output signal (Pin 16) at a constant level. Therefore the sync level of the demodulated video signal is the criterion for a fast charge/discharge of the AGC capacitor. The AGC control voltage at Pin 2 is transferred to an internal control signal and is fed to the tuner AGC to generate the tuner AGC current on Pin 4 (open collector output). Take over point of the tuner AGC can be adjusted at Pin 1 by a potentiometer or an external DC voltage (from interface circuit or microprocessor).

FPLL, VCO and AFC

The FPLL circuit (frequency phase locked loop) consists of a frequency and phase detector to generate control voltage for the VCO tuning. In the locked mode the VCO is controlled by the phase detector and in unlocked mode the frequency detector is superimposed. The VCO operates with an external resonance circuit (L and C parallel) and is controlled by internal varicaps. VCO control voltage at Pin 27 (loop filter) is also converted to a current and represents the AFC output signal at Pin 20.

A practicable VCO alignment of the external coil is the adjustment to zero AFC output current at Pin 20. At centre frequency the AFC output current is equal to zero. The optional potentiometer at Pin 26 allows an offset compensation of the VCO phase for improved sound quality (fine adjustment). Without a potentiometer (open circuit at Pin 26) this offset compensation is not active.

The oscillator signal passes a phase shifter and supplies the in–phase signal (0) and the quadrature signal (90) of the generated picture carrier.

AFC Switch

The AFC output signal at Pin 20 can be controlled by a switching voltage at Pin 22. It is possible to switch off the AFC.

Video Demodulation and Amplifier

The video IF signal, which is applied from the gain controlled IF amplifier, is multiplied with the inphase component of the VCO signal. The video demodulator is designed for low distortion and large bandwidth. The demodulator output signal passes an integrated low pass filter for attenuation of the residuel vision carrier and is fed to the video amplifier. The video amplifier is realized by an operational amplifier with internal feedback and 8 MHz bandwidth. An additional noise clipping is provided. The video signal is fed to VIF–AGC and to the video output buffer. This amplifier offers easy adaption of the sound trap and sound filter. For nominal video IF modulation the video output signal at Pin 16 is 1.5 V (peak to peak value).

Sound IF Limiter Amplifier

The intercarrier signal coming from the sound filter is fed to a 7–stage limiter amplifier. This guarantees high input sensitivity and excellent AM suppression.

PLL – FM Demodulator

The alignment–free "Phase–Locked–Loop" (PLL) FM demodulator covers a wide frequency range of 4.5 MHz up to 6.5 MHz with excellent noise performance. The linear voltage to frequency characteristic results in low harmonic distortion. The free running frequency of the internal VCO circuit is about 5.5 MHz.

Audio amplifier, deemphasis and mute switch

The demodulated FM signal is led via deemphasis and buffered to Pin 7. Deemphasis low pass consists of internal 5 k series resistor and external capacitor at Pin 13. The FM muting is possible by switching Pin 13 to ground.

SCART – Video Processing

A full SCART interface is included. The video SCART switch has two inputs (for signals from video demodulator and SCART socket) and two outputs (SCART socket and main video output). The video demodulator output signal (Pin 16: 1.5 V) and the sound trap video input (Pin 17: 1V) are connected by a DC–coupled sound trap. A 6 dB amplifier applies permanently the video signal to the SCART output (Pin 14: 2 V). The AC–coupled SCART input signal (Pin 12: 1 V) is clamped internally and fed to the video switch. The selected video signal passes a 6 dB buffer amplifier with low output resistance. For nominal signal conditions the video output signal at Pin 15 is 2 V (peak to peak value).

SCART – audio processing

The audio SCART switch has inputs for the demodulated AF signal and the external AF signal from SCART socket. The demodulated AF signal permanently is available at Pin 7. The selected AF signal is fed to volume control.

SCART control switch

The common selector switch for video and audio signals is controlled by a DC voltage at Pin 18. In the "internal mode" the demodulated signals are selected. For the selection of video/audio signals supplied via SCART socket the "external mode" has to be switched on.

Internal voltage stabilizer

The internal bandgap reference ensures constant performance independant of supply voltage and temperature.

Ordering Information

Extended Type Number	Package	Remarks
TDA 4462 – ASD	SDIP 28	
TDA 4462 – AFLG3	SO 28	delivery in taped form

Preliminary Information

Pin description

Pin	Symbol	Function
1	V_{top}	Tuner AGC – take over point
2	C_{AGC}	VIF–AGC (time constant)
3	GND	Ground
4	I_{tun}	Tuner AGC output current
5, 6	$V_{i,VIF}$	VIF input (symmetrical)
7	$v_{o,AF}$	Audio output – SCART
8	$v_{i,AF}$	Audio input – SCART
9	V_{vol}	Volume control
10	$v_{o,AF}$	Audio output
11	C_{dec}	Decoupling capacitor
12	$v_{i,vid}$	Video intput – SCART
13	C_{dem}	Deemphasis and mute switch
14	$v_{o,vid}$	Video output – SCART
15	$v_{o,vid}$	Video output
16	$V_{o,vid}$	Video demodulator output
17	$V_{i,vid}$	Video input – sound trap
18	Vsw	Mode selection SCART switch
19	GND	Ground
20	V_{AFC}	AFC output
21	$v_{i,SIF}$	FM sound IF input
22	V_{sw}	AFC control switch
23, 24	V_{vco}	VCO circuit (FPLL)
25	V_s	Supply voltage
26	R_{comp}	Offset compensation
27	LF	Loop filter
28	C_{ref}	Internal reference voltage
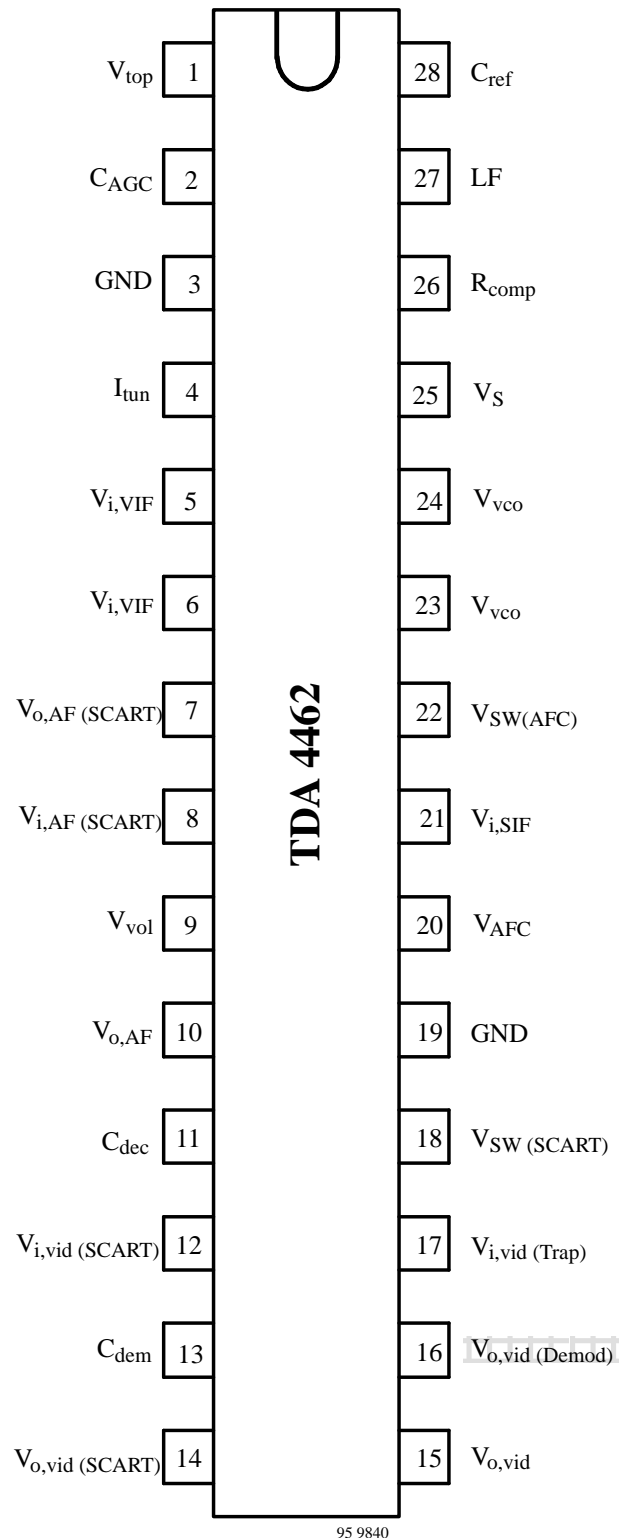
Figure 2.

Absolute Maximum Values

Reference point Pin 3 (19), unless otherwise specified

Parameters	Symbol	Value	Unit
Supply voltage SDIP 28 package Pin 25 SO 28 package	V_s	9.0 6.0	V V
Supply current Pin 25	I_s	80	mA
Power dissipation $V_S = 9\ V$ $V_S = 6\ V$	P	720 400	mW mW
Output currents Pin10, 15, 18	I_{out}	5	mA
External voltages	V_{ext}	+ 4.5	V
		+ 3.5	V
		+ 13.5	V
		V_S	V
Junction temperature	T_{junc}	+125	°C
Storage temperature	T_{stor}	−25 to +125	°C
Electrostatic handling *) all Pins	V_{ESD}	tbf	V

*) equivalent to discharge a 200 pF capacitor through a 0 resistor

Operating Range

Parameters	Symbol	Value	Unit
Parameters	Symbol	Value	Unit
Supply voltage range SDIP 28 package Pin 25 SO 28 package	V_S	4.5 to 9.0 4.5 to 6.0	V V
Ambient temperature	T_{amb}	−10 to +85	°C

Thermal Resistance

Parameters	Symbol	Value	Unit
Parameter	Symbol	Value	Unit
Thermal resistance junction–ambient when soldered to PCB SDIP 28 package SO 28 package	R_{thja}	55 75	K/W K/W

Preliminary Information

Electrical Characteristics

$V_s = +5V$, $T_{amb} = +25°C$; reference point pin 3 (19), unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
DC–supply:	Pin 25					
Supply voltage SDIP 28 package SO 28 package		V_s	4.5 4.5	5.0 5.0	9.0 5.5	V V
Supply current		I_s		66	80	mA
VIF–input:	Pin 5–6					
Input sensitivity,RMS value	for FPLL locked	$v_{i,VIF}$		80	120	µV
Input resistance	see Note 1	R_{in}		1.2		k
Input capacitance	see Note 1	C_{in}		2		pF
IF–AGC:	Pin 2					
IF gain control range		G_v	60	65		dB
AGC capacitor		C_{AGC}		2.2		µF
Tuner–AGC:	Pin 1, 4 see Note 2					
Available tuner-AGC current		I_{tun}	1	2	4	mA
Allowable output voltage		V_{tun}	0.3		13.5	V
IF slip – tuner AGC	current I_{tun}: 10% to 90%	G_{IF}		8	10	dB
IF input signal for minimum take over point	$R_{top} = 10$ k ($V_{top} = 4.5$ V)	v_{in}			4	mV
IF input signal for maximum take over point	$R_{top} = 0$ ($V_{top} = 0.8$ V)	v_{in}	40			mV
Variation of the take over point by temperature	$T_{amb} = 55°C$ VIF–AGC: $G_v = 46$ dB	v_{in}		2	3	dB
FPLL and VCO:	Pin 23, 24, 26, 27					
Max. oscillator frequency	for carrier generation	f_{vco}	70			MHz
Vision carrier capture range	$f_{vco} = 38.9$ MHz $C_{vco} = 6.8$ pF	f_{cap}	1.5	2		MHz
Oscillator drift (free runing) as function of temperature	see Note 3 $T_{amb} = 55°C$, $C_{vco} = 6.8$ pF, $f_{vco} = 38.9$ MHz	$f/_T$			–0.3	%
Video demodulator output:	Pin16					
Output current–source	DC and AC	I_{out}	4		5	mA
–sink	DC and AC		2		3	mA
Output resistance	see Note 1	R_{out}			100	
Video output signal	peak to peak value	$v_{o,vid}$	1,35	1,5	1,65	V
Sync level		V_{sync}		1.8		V
Zero carrier level (Ultra white level)	AGC voltage $V_2 = 3$ V	V_{DC}		3.3		V

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Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Supply voltage influence on the ultra white level		$V/_V$		1		%/V
Video bandwidth (–3dB)	R_L 1 k, C_L 50 pF	B	6	8		MHz
Video frequency response over the AGC range		B			2.0	dB
Differential gain error		DG		2	5	%
Differential phase error		DP		2	5	deg
Intermodulation 1.07MHz related to colour carrier	test signal unmodulated, with picture carrier: 0 dB colour carrier: – 6 dB sound carrier: – 24 dB	a_{IM}	52			dB
Video signal to noise ratio	weighted , CCIR–567	$S/_N$	56	60		dB
Residual vision carrier fundamental wave 38.9 MHz and second harmonic 77.8 MHz		v_{res}		2	10	mV
Ripple rejection, Pin 25/ 16	see Note 1	RR	35			dB
AFC output:	Pin 20					
Control slope		$I/_f$		0.7		A/kHz
Frequency drift by temperature	related to the picture carrier frequency			0.25	0.6	%
Output voltage upper limit lower limit		V_{AFC}	V_s–0.4		0.4	V V
Output current		I_{AFC}		0.2		mA
AFC switch:	Pin 22					
Control voltage: AFC "off" AFC "on"	see Note 4	V_{sw}	0 2.0		0.8 V_s	V V
Switching current		I_{sw}		100		A
Video input – sound trap:	Pin 17					
Input resistance	see Note 1	R_{in}		3		k
Input capacitance	see Note 1	C_{in}		2.0		pF
Internal DC bias voltage (clamping voltage)		V_{DC}		1.7		V
Video input signal (CVBS)	peak–to–peak value	$v_{i,vid}$		1		V
Video output – SCART:	Pin 14					
DC output voltage		V_{DC}		1.25		V
Voltage gain, pin 17 pin 14		G_v		6		dB
Video output signal (CVBS)	peak–to–peak value v_{in} = 1V Pin 17	$v_{o,vid}$		2		V
Video input – SCART:	Pin 12					
Input resistance	see Note 1	R_{in}		25		k

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Input capacitance	see Note 1	C_{in}		2.0		pF
Internal DC clamping voltage		V_{DC}		1.7		V
Video input signal	peak to peak value	$v_{i,vid}$		1		V
Video output:	Pin 15					
Output resistance		R_{out}			100	
Output current - source - sink	DC and AC	I_{out}	4 2		5 3	mA mA
DC output voltage		V_{DC}		1.25		V
Voltage gain: Pin 17 Pin 15 Pin 12 Pin 15		G_v		6 6		dB dB
Video output signal	peak to peak value, $v_{in} = 1$ V	v_{out}		2		V
Video bandwidth (–3dB)	R_L 1 k, C_L 50 pF	B	8	10		MHz
Cross talk attenuation	$f_{in} = 50$ Hz – 10 MHz	a		55		dB
FM sound IF input:	Pin 21					
Input limiting voltage, RMS value	AF output signal at Pin 7: –3 dB	$v_{i,SIF}$			150	mV
DC input voltage		V_{DC}		1.7		V
Input resistance	see Note 1	R_{in}		600	750	
Input capacitance	see Note 1	C_{in}		1.5		pF
FM – PLL:						
Free–running frequency		f_{vco}		5.5		MHz
Oscillator drift (free running) as function of temperature	T = 55 °C	f_{vco}		500		kHz
Oscillator shift (free running) as function of supply voltage	4.5 V < V_s < 9.0 V	f_{vco}		200		kHz
Capture range of PLL		f_{cap}	1.4	1.9		MHz
Holding range of PLL		f_{hold}	2.0	3.0		MHz
Audio output:	Pin 10					
DC output voltage		V_{DC}		2.2		V
Output resistance		R_{out}		100		
AC output peak current		i_{AC}			1.5	mA
DC output current		I_{DC}			–2.0	mA
AF output voltage, RMS value	$v_{in} = 10$ mV, f = 5.5 MHz, FM–dev. = 50 kHz, $f_{mod} = 1$ kHz	$v_{o,AF}$		500		mV

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Total harmonic distortion	v_{in}=10 mV, f = 5.5 MHz, FM–dev. = 50 kHz, f_{mod} = 1 kHz	THD		0.1	0.3	%
AM suppression	v_{in} = 10 mV, f = 5.5 MHz, f_{mod}=1 kHz, <u>reference signal:</u> FM–dev. = 50 kHz <u>test signal:</u> m = 30 %	a_{AM}	46	66		dB
Supply voltage ripple rejection	V_{RR} < 200 mV, f = 70 Hz	RR		20		dB
Audio output – SCART:	Pin 7					
DC output voltage		V_{DC}		2.3		V
AF output voltage		$v_{o,AF}$		500		mV
Output resistance		R_{out}		140		
Audio input – SCART:	Pin 8					
Input resistance		R_{in}		50		k
Internal DC bias voltage		V_{DC}		3.0		V
AF input signal		$v_{i,AF}$			750	mV
Deemphasis capacitor and mute switch:	Pin 13					
Value of deemphasis capacitor		C_{dem}		10		nF
Control voltage for "mute off"	AF "on", see Note 5	V_{sw}	2.0		V_s	V
Control voltage for "mute on"	AF "off"	V_{sw}	0		0.8	V
Decoupling capacitor:	Pin 11					
Value of decoupling capacitor		C_{dec}		2.2		F
Volume control:	Pin 9					
AF control range		AF		80		dB
Control voltage -minimal volume -maximal volume		V_{ctl}	0	4	V_s	V V
Mode selection – SCART switch:	Pin 18					
Control voltage: RF mode VCR mode	see Note 6	V_{sw}	2.0 0		V_s 0.8	V V
Switching current		I_{sw}		100		A

Preliminary Information

Notes:

1.	This parameter is given as an application information and not tested during production.

2.	Adjustment of turn over point (delayed tuner AGC) with external resistor R_{top} or external voltage V_{top} possible.

3.	The oscillator drift is related to the picture carrier frequency, at external temperature–compensated LC circuit

4.	Without control voltage at pin 22 the "AFC on" mode is automatically selected

5.	Without external control voltage at pin 13 mute function is not active

6.	Without control voltage at pin 18 the "internal mode" automatically is switched on (demodulated signals are selected)
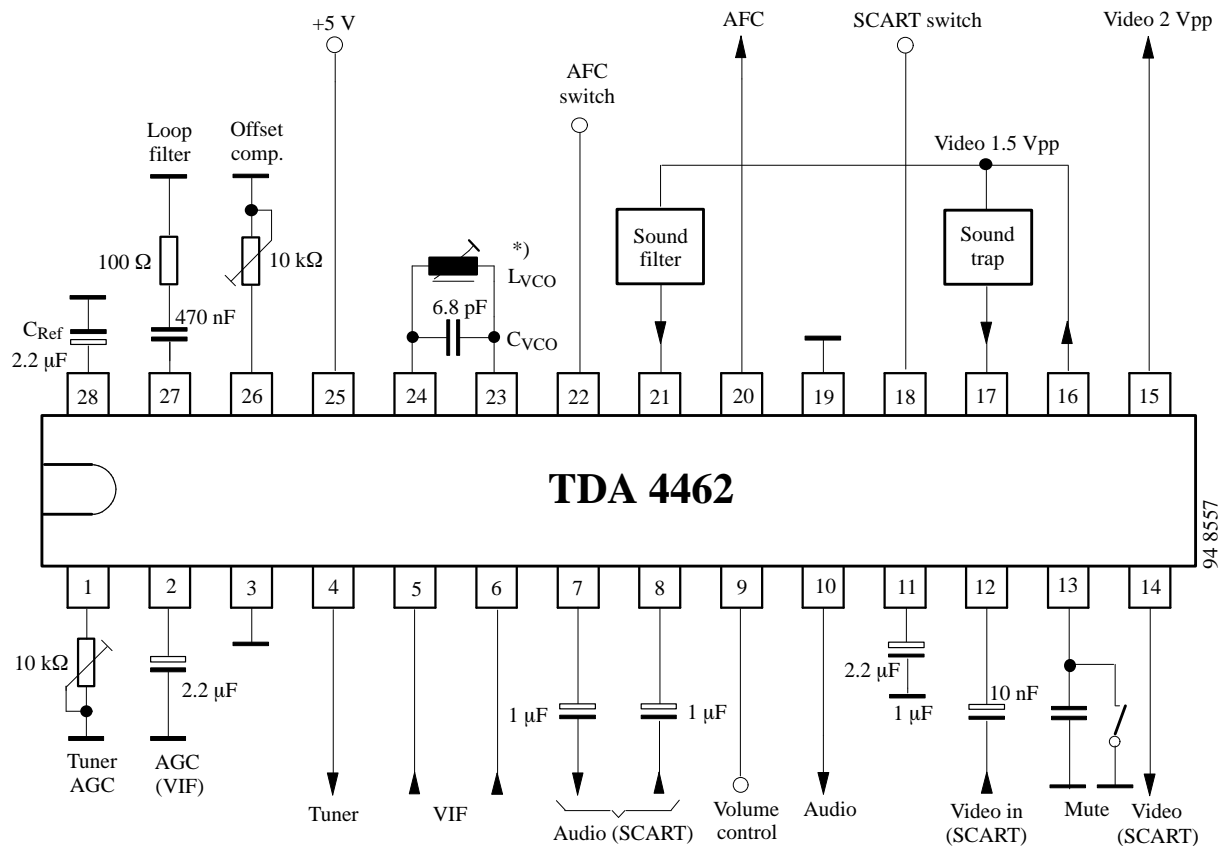
*) External L/C circuit (VCO: 38.9 MHz) with TOKO coil (9 turns, 0.12mm)

Figure 3. Test circuit
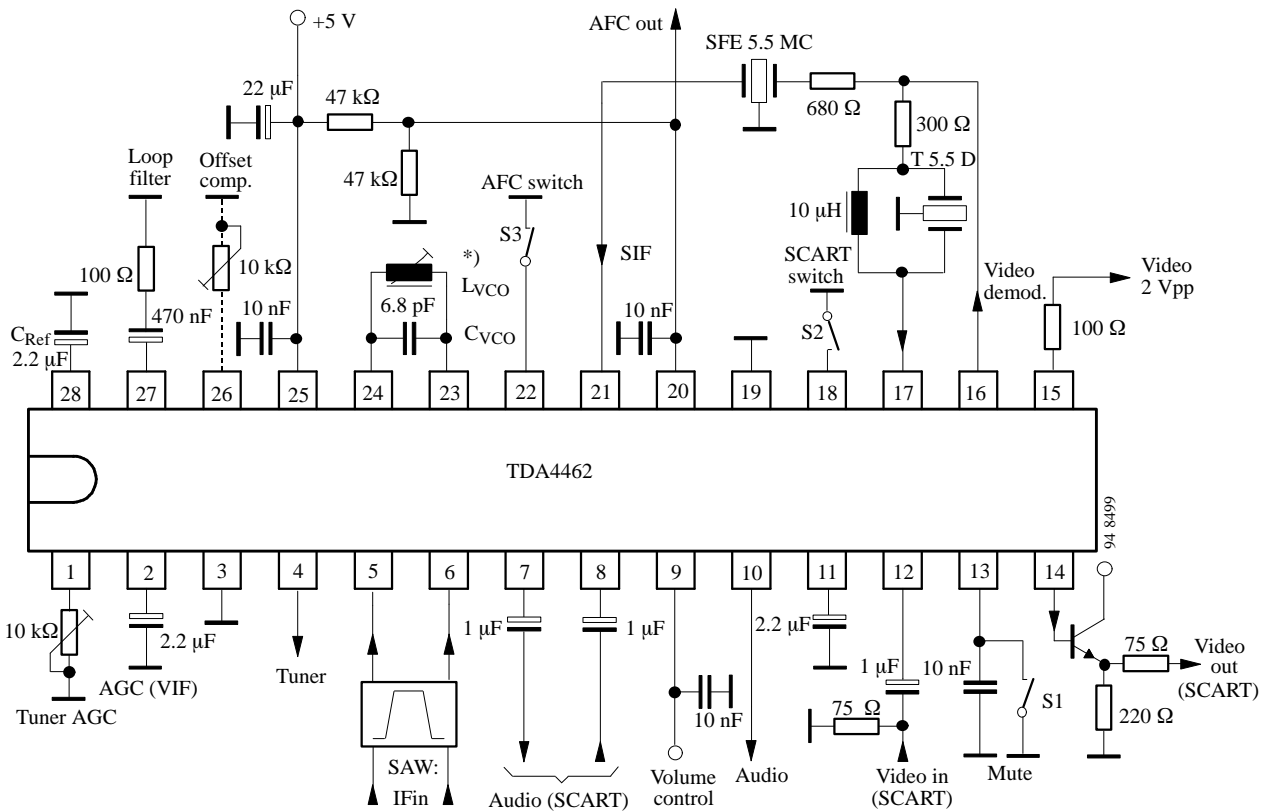
Figure 4. Basic application circuit

Internal Pin Configuration
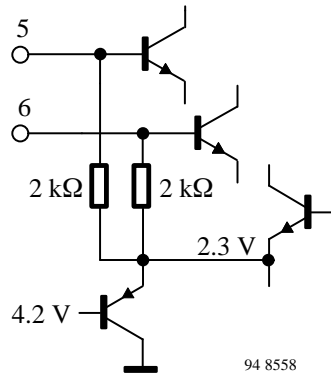
Figure 5. Video IF input (Pin 5–6)
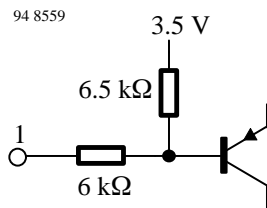
Figure 6. Take over point – Tuner AGC (Pin 1)
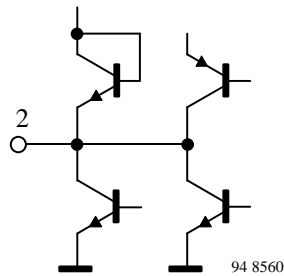
Figure 7. Time constant – VIF AGC (Pin 2)
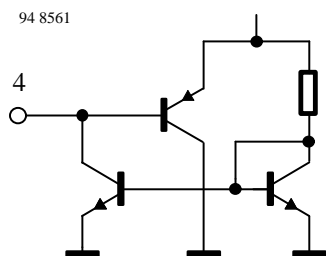
Figure 8. Tuner AGC current output (Pin 4)
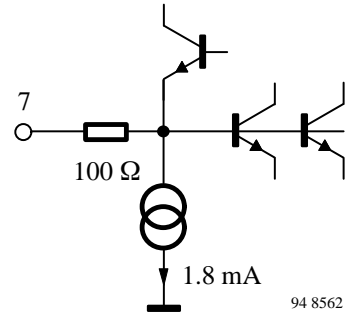
Figure 9. Audio output – SCART (Pin 7)
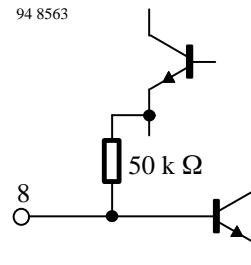
Figure 10. Audio input – SCART (Pin 8)
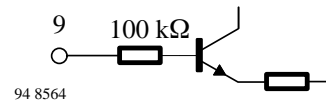
Figure 11. Volume control (Pin 9)
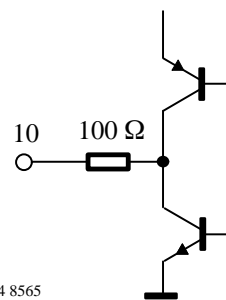
Figure 12. Audio output (Pin 10)

94 8566
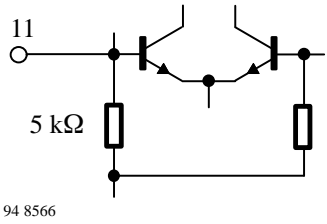
Figure 13. Decoupling capacitor (Pin 11)

94 8570

Figure 17. Video output (Pin 15)

94 8567

Figure 14. Video input – SCART (Pin 12)

94 8571
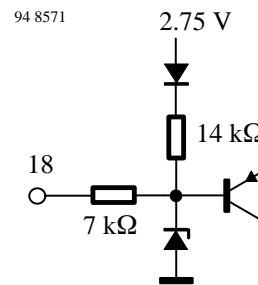
Figure 18. Mode selection – SCART switch (Pin 18)

94 8568

Figure 15. Deemphasis and mute switch (Pin 13)

94 8572
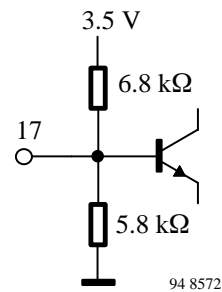
Figure 19. Video input – sound trap (Pin 17)

94 8569

Figure 16. Video output – SCART (Pin 14)

94 8573
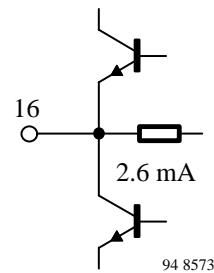
Figure 20. Video demodulator output (Pin 16)

Preliminary Information
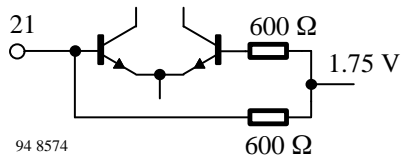
Figure 21. FM sound IF input (Pin 21)
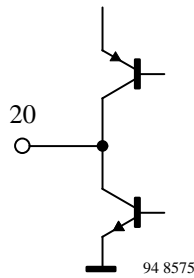
Figure 22. AFC output (Pin 20)
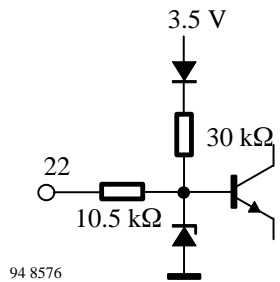
Figure 23. AFC control switch (Pin 22)
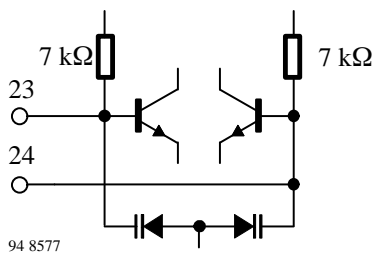
Figure 24. VCO circuit (Pin 23–24)
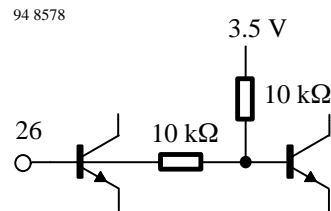
Figure 25. Offset compensation (Pin 26)
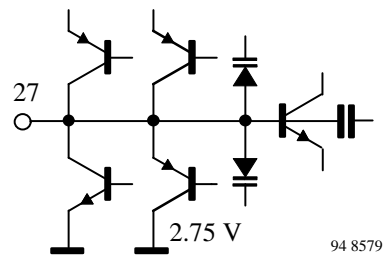
Figure 26. Loop filter (Pin 27)
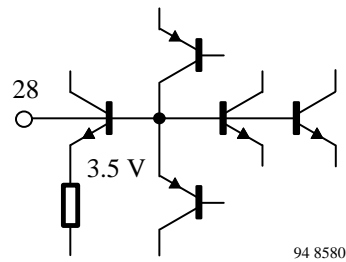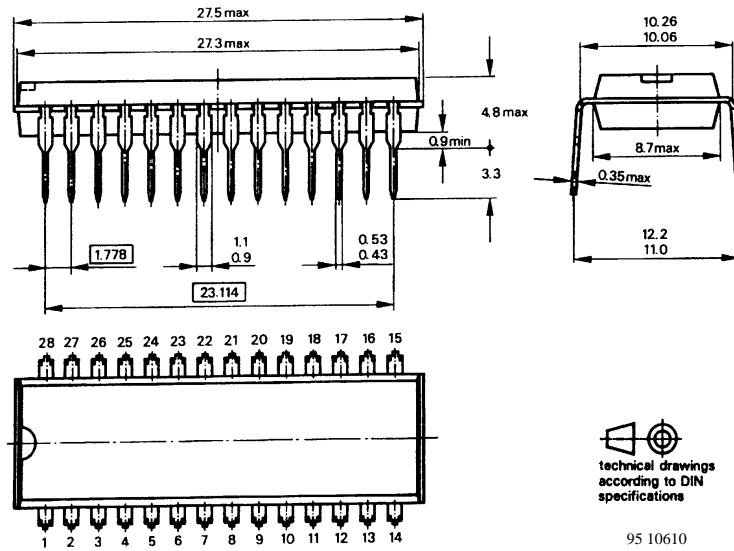
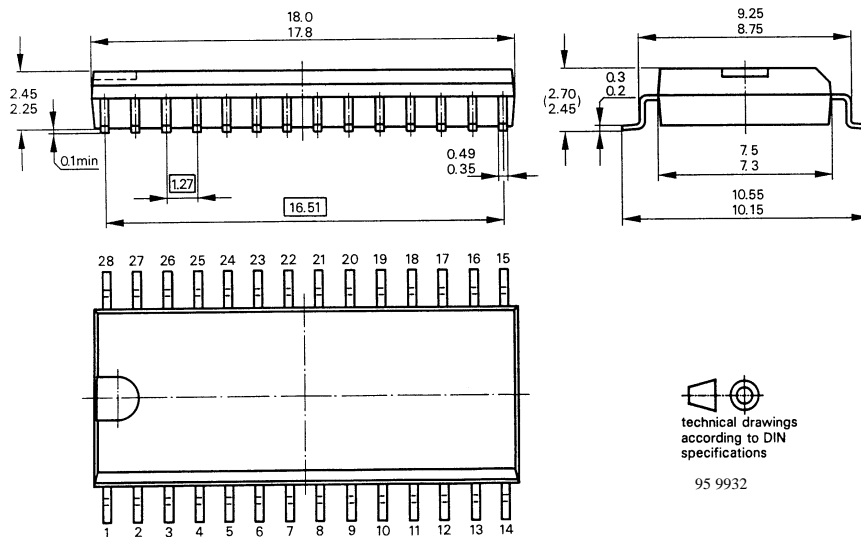Figure 27. Internal reference voltage (Pin 28)

Dimensions in mm

Package: 28 pin shrink–dual–inline–plastic (SDIP28) :

technical drawings
according to DIN
specifications

95 10610

Package: 28 pin small–outline–plastic (SO28) :

95 10610

technical drawings
according to DIN
specifications

95 9932

Preliminary Information

Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC TELEFUNKEN microelectronic GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC TELEFUNKEN microelectronic GmbH semiconductor division has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.